VERTICAL FIN-FET MOS DEVICES

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates generally to semiconductor devices, more particularly to MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) devices, and still more particularly to vertical MOSFETs.

BACKGROUND OF THE INVENTION

[0002] In 1965, Dr. Gordon Moore, then Director of Research and Development for Fairchild Semiconductor, made the observation that the number of transistor devices per integrated circuit had been doubling every couple of years since the creation of the first integrated circuits in the late 1950's and that he expected the trend to continue for the foreseeable future. This observation was dubbed "Moore's Law" by the trade press. Now almost 40 years later, despite numerous dire predictions of fundamental obstacles, unrelenting industry efforts towards every-increasing semiconductor density have effectively affirmed Dr. Moore's prophetic observation, and the trend is still expected to continue unabated for the foreseeable future. The process of reducing semiconductor device size to increase integrated circuit density is generally referred to as "scaling".

[0003] Ongoing scaling efforts of semiconductor MOS (Metal-Oxide-Semiconductor) devices not only contribute to higher integrated circuit packing density, but also improve integrated circuit performance. As the scaling process proceeds towards the physical limits of currently available MOS technologies and techniques, new technologies and techniques are developed to further decrease device size and increase device performance. As MOS device size decreases, tremendous challenges arise in a variety of areas, including source/drain contact resistance and current carrying capacity. In these two areas at least, extremely small size tends to work against performance.

[0004] One approach that has been employed to improve current carrying capacity of extremely small-geometry FETs is the creation of "double gate" (also referred to as dual-gate herein) transistors. In principle, double-gate transistors act something like two transistors in parallel, thereby improving current flow between source and drain. Two major types of

double-gate transistors have been demonstrated: the planar double-gate transistor and the double-gate Fin-FET.

[0005] The planar double-gate FET is not unlike a conventional single gate transistor in that it has a horizontal "planar" transistor body with a source and drain at each end and a channel therebetween. Unlike single-gate transistors, however, the planar double-gate FET has a second gate below the transistor body effectively creating a second, parallel channel between the source and drain. However, there is considerable process complexity involved in forming the second, buried gate and in connecting to it, and the planar double-gate transistor is not significantly different from conventional planar transistor structures in terms of its ability to be scaled. Such planar devices are rapidly approaching the physical limits of scaling.

[0006] The double-gate Fin-FET employs thin vertical silicon "fins" that act as the transistor body. Horizontally opposed ends of the fin act as source and drain. The gate structure is formed around the fin in an inverted "U" configuration such that the fin has parallel gates formed along both vertical sidewalls thereof. As in the planar double-gate transistor, the double-gate Fin-FET improves current flow between source and drain by effectively creating parallel channels therebetween. Current flows horizontally through the fin between source and drain when the double gate is appropriately biased. Because the transistor body of the Fin-FET is a thin vertical structure, there can be considerable space savings over similar planar devices. Series resistance in Fin-FETs is a significant problem, however.

SUMMARY OF THE INVENTION

[0007] The present inventive technique produces high-density, vertical Fin-FET devices with low contact resistance by means of vertical silicon "fins" that act as the transistor body. Doped source and drain regions are formed at the bottoms and tops, respectively, of the fins. Gate structures are formed along sidewalls of the fins, spanning the vertical distance between the source and drain regions and separated from the fins by thin gate insulators. Current flows vertically through the channel region between the source and drain regions when an appropriate bias is applied to the gates. Through the use of selective

doping, both nFET and pFET variants of the inventive vertical Fin-FET device are easily formed on the same substrate. Preferably, the substrate is an SOI (silicon-on-insulator) wafer, but any suitable substrate or portion thereof having a silicon layer formed over an insulator layer (e.g., buried oxide layer – "BOX") could be employed.

[0008] The basic structure of the inventive vertical Fin-FET device is characterized by at least one vertical semiconductor fin disposed on an insulator layer. Doped source and drain regions are formed in bottom and top portions of the fin(s) and gate conductors are disposed along vertical sidewalls of the at least one semiconductor fin. The gate conductors are space away from the fins by thin gate insulators.

[0009] According to an aspect of the invention, the gate conductors span a vertical distance between the source region and drain region of the fin(s). Since gate conductors are disposed on both sides of the fin(s), the vertical Fin-FET is essentially a dual-gate device. When an appropriate biasing voltage is applied to the gate conductors, channels form between the source and drain regions adjacent to each gate, effectively creating parallel channels and improving the current carrying capacity of the vertical Fin-FET as compared to single-gate devices.

[00010] Generally speaking, source conductors contact the source regions on both sides of the fins. Source contacts (typically metal) are employed to connect to the source conductors, drain contacts connect to the drain regions and gate contacts connect to the gate conductors.

[00011] According to an aspect of the invention, the gate connections can be made either separately or in common. Providing separate gate contacts that connect to the gate conductors on opposite sides of a fin yields a multi-gate vertical Fin-FET whereby each of the gates can be separately controlled. Connecting to the gate conductors on opposite sides of a fin in parallel with a single gate contact yields a double-gate vertical Fin-FET with enhanced drive capability.

[00012] According to another aspect of the invention, the source contact can connect to the source conductor on one side of the fin only in a "single-source" variant of the vertical Fin-FET.

[00013] Multi-Fin versions of the vertical fin-FET are readily formed by creating multiple fins and connecting them in parallel such that the source conductors are all connected together, the drain regions are all connected together and the gate conductors are all connected together. Alternatively, the gates can be connected such that two gate contacts are provided where one gate contact connects to all of the gate conductors on one side of each fin and the other gate contact connects to all of the gate conductors on the other side of each fin.

[00014] According to another aspect of the invention, a "fat-drain" variation improves drain contact resistance. In this variation, the drain contact is "widened" to over extend the fin laterally.

[00015] By selective doping, nFET and pFET devices are readily created on the same substrate. For nFET devices, the source regions, drain regions, gate conductors and source conductors are all n+ doped. For pFET devices, the source regions, drain regions, gate conductors and source conductors are all p+ doped.

[00016] Any number of pFET and/or nFET devices can be created, and multi-Fin devices can be created using the same process steps as single-fin devices. This permits any combination of single-fin and/or multi-fin pFET and/or nFET devices to be formed on a single substrate using essentially the same process steps. These devices can be parts of CMOS circuits or non-complementary circuits and can be part of a large integrated circuit device.

[00017] One suitable method for forming the vertical fin-FET device can be summarized as a series of processing steps as follows:

(1) provide a semiconductor substrate having a semiconductor layer disposed over an insulator layer;

(2) form vertical semiconductor fins on top of the insulator layer by etching parallel trenches through the semiconductor layer down to the insulator layer;

(3) selectively deposit doped source conductors at the bottoms of the trenches such that the doped conductors contact bottom portions of the fins;

(4) form source insulators over the doped conductors;

(5) form gate insulators along sidewalls of the trenches;

(6) thermally drive dopants from the doped conductors into bottom portions of the fins to create source regions;

(7) form gate conductors along vertical sidewalls of the fins spaced away the fins by the gate insulators;

(8) dope top portions of the fins to form drain regions therein;

(9) form sidewall spacers along exposed sidewalls of the trenches, fins and gate conductors;

(10) etch back the source insulators to expose the underlying doped source conductors;

(11) form silicide in exposed portions of the source and gate conductors;

(12) fill the trenches with an oxide trench-fill and planarize;

(13) form metal source, drain and gate contacts by Damascene processes of selective etching, metal fill, and chem-mech polishing.

BRIEF DESCRIPTION OF THE DRAWINGS

[00018] These and further features of the present invention will be apparent with reference to the following description and drawing, wherein:

[00019] Figures 1-10 are cross-sectional diagrams of a vertical Fin-FET semiconductor structure on an SOI substrate at a series of sequential processing steps, in accordance with the invention.

[00020] Figure 11 is a plan view of a vertical Fin-FET semiconductor structure with source, drain and gate contacts, in accordance with the invention.

[00021] Figures 12-14 are different cross sectional views of the vertical Fin-FET semiconductor structure of Figure 11, in accordance with the invention.

[00022] Figure 15 is a cross-sectional view of a "fat drain" embodiment of a vertical Fin-FET semiconductor structure, in accordance with the invention.

[00023] Figure 16 is a plan view of a "single-side source" embodiment of a vertical Fin-FET semiconductor structure, in accordance with the invention.

[00024] Figure 17 is a plan view of a "multi-gate" embodiment of a vertical Fin-FET semiconductor structure, in accordance with the invention.

[00025] Figure 18 is a cross-sectional view of a "multi-fin" embodiment of a vertical Fin-FET semiconductor structure, in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

[00026] The present inventive technique produces high-density, vertical Fin-FET devices with low contact resistance by forming tall, thin vertical silicon "fins" that act as the transistor body. Appropriately doped source and drain regions are formed at the bottoms and tops, respectively, of the fins and gate structures are formed along sidewalls of the fins, overlapping the doped source and drain regions, thereby creating a vertical channel region in the fin between the source and drain regions. Current flows vertically through channels that form in the channel region adjacent to the gate structures and extending between the source and drain regions when an appropriate bias is applied to the gates. Through the use of selective doping, both nFET and pFET variants of the inventive vertical Fin-FET device are easily formed on the same substrate. Preferably, the substrate is an SOI (silicon-on-insulator) wafer, but any suitable substrate or portion thereof having a silicon layer formed over an insulator layer (e.g., buried oxide layer – "BOX") could be employed. Preferably, an SOI substrate having a nitride layer overlying a silicon layer that in turn overlies a buried oxide layer (BOX) is employed.

[00027] A preferred embodiment of a method for forming vertical Fin-FET semiconductor structures can be summarized as: (1) Forming tall, thin vertical semiconductor

(silicon) "fins" on top of an insulator layer in a suitable substrate (e.g. SOI), e.g., by etching parallel trenches through the silicon layer down to the insulator layer (e.g, BOX); (2) selectively depositing n+ and/or p+ doped polysilicon conductors at the bottoms of the trenches (as appropriate to the type of FinFET devices being formed: nFET and/or pFET) such that the doped polysilicon conductors contact bottom portions of the fins; (3) forming an HDP oxide insulating layer over the polysilicon; (4) effecting appropriate channel doping (in the "fin") using conventional masking and implantation techniques; (5) forming gate insulators along sidewalls of the trenches and thermally "driving" the polysilicon dopants into bottom portions of the fins; (6) forming gate conductors on the sides of the fins (with the gate insulators separating the gate conductors from the fins); (7) Selectively implanting n+ and/or p+ dopants (as appropriate to the type of FinFET devices being formed: nFET and/or pFET) into top portions of the fins to form drain regions therein; (8) depositing nitride and etching back to form sidewall spacers; (9) etching back the HDP oxide to expose the underlying doped polysilicon source conductors and forming silicide in exposed portions of the source and gate conductors; (10) filling the trenches with an oxide trench-fill and planarizing via CMP (chem-mech polishing); and (11) forming metal source, drain and gate contacts by Damascene processes of selective etching, metal fill, and chem-mech polishing.

[00028] It should be noted that in the ensuing detailed description of the preferred embodiment(s) of the invention, drawing features are not necessarily to scale and should be interpreted as being merely schematically representative of the relationships between the structures and features depicted.

[00029] Figure 1 is a cross-sectional diagram of an SOI wafer substrate 100 on which n-channel and p-channel vertical Fin-FETs are to be formed, in accordance with the invention. Preferably, the wafer substrate structure has a bulk silicon layer 2 over which a buried oxide layer (BOX) 4 is formed. Overlying the buried oxide layer 4 is a single-crystal silicon layer 6. A nitride dielectric layer (e.g., SiN) 8 overlies the silicon layer 6. Preferably the silicon layer 6 is 50-200 nanometers (nM – 10^{-9} meters) in thickness, but with further device scaling, thinner layers may be appropriate.

[00030] Figure 2 is a cross-sectional diagram of a wafer substrate 200 representative of the wafer substrate 100 of Figure 1 after etching to form well-defined, parallel trenches 10A, 10B, 10C and 10D through the nitride layer 8 and silicon layer 6 down to the BOX layer 4.

Trenches 10A and 10B define a first fin 12A therebetween, which will become the body of an nFET transistor (generally indicated in the Figure as "nFET"). The first fin 12A has a nitride "cap" 14A. Trenches 10C and 10D define a second fin 12B therebetween, which will become the body of a pFET transistor (generally indicated in the Figure as "pFET"). The second fin 12B also has a nitride "cap" 14B. Trenches 10B and 10C define a spacer structure therebetween comprising a silicon base 16B with a nitride cap 16A. Preferably, the fins 12A and 12B are 10-20 nM wide, but with further device scaling, smaller widths may be appropriate. The heights of the fins 12A and 12B are equal to the thickness of the silicon layer 6, preferably 50-200 nM.

[00031] Figure 3 is a cross-sectional diagram of a wafer substrate 300 representative of the wafer substrate 200 of Figure 2 after a process of forming n+ doped polysilicon source conductors 18A at the bottoms of trenches 10A and 10B, respectively, and forming p+ doped polysilicon source conductors 18C and 18D at the bottoms of trenches 10C and 10D, respectively. Preferably, the source conductors 18A and 18B are formed by masking off the inchoate "pFET" device (generally indicated in the Figure as "pFET") and depositing n+ doped polysilicon in trenches 10A and 10B (generally associated with the inchoate "nFET" device generally indicated in the Figure as "nFET") and etching back such that the n+ source conductors 18A and 18B generally uniformly fill the trenches 10A and 10B to a uniform depth, contacting the fin 12A only at a bottom portion thereof. Then the mask is removed and source conductors 18C and 18D are formed in similar fashion by masking off the inchoate "nFET" device and depositing p+ doped polysilicon in trenches 10C and 10D (generally associated with the inchoate "pFET" device) and etching back such that the p+ source conductors 18C and 18D generally uniformly fill the trenches 10C and 10D to a uniform depth, contacting the fin 12B only at a bottom portion thereof. Those of ordinary skill in the art will immediately understand that the order of processing (i.e., "nFET first" as described herein where n+ source conductors 18A and 18B are formed first or or "pFET first" where p+ source conductors 18C and 18D are formed first) is not critical, and the inventive technique is readily adapted to either order of processing. Further, if only nFET devices or pFET devices are required, some intermediate steps can be eliminated.

[00032] Figure 4 is a cross-sectional diagram of a wafer substrate 400 representative of the wafer substrate 300 of Figure 3 after forming HDP oxide layers 20A, 20B, 20C and 20D on top of source conductors 18A, 18B, 18C and 18D, respectively. Preferably, the HDP

oxide layers are formed by an HDP (High-density plasma) oxide deposition process followed by a sidewall etch. Assuming that the inchoate nFET and pFET transistors (generally indicated in the Figure as "nFET" and "pFET", respectively) are part of a larger, integrated semiconductor device, those of ordinary skill in the art will immediate appreciate and understand that any required gas phase doping and/or well implantation can be performed at this point using appropriately patterned masks.

[00033] Figure 5 is a cross-sectional diagram of a wafer substrate 500 representative of the wafer substrate 400 of Figure 4 after forming gate insulators 22 and "driving in" source dopants from the source conductors 18A, 18B, 18C and 18D into the fins 12A and 12B to form source regions 26A and 26B, respectively, therein. Preferably, the gate insulators 22 are formed on exposed silicon sidewalls of the trenches 10A, 10B, 10C and 10D (including exposed sidewalls of the fins 12A and 12B) via a thermal oxide formation process. This same thermal process causes thermal diffusion "drive in" of the n+ source dopant in source conductors 18A and 18B into a bottom source-region portion 26A of the first fin 12A and of the p+ source dopant in source conductors 18C and 18D into a bottom source-region portion of the second fin 26B. If desired, additional heating can be employed to continue the source "drive in" thermal diffusion process. As shown in the Figure, the "driven in" source diffusion from opposite sides of the fins tends to overlap and mix (shown as overlapping curved lines in the source regions 26A and 26B). The HDP oxide layers 20A, 20B, 20C and 20D should be thin enough that the drive-in process causes the source-regions 26A and 26B to reach higher in the fins 12A and 12B than the upper surfaces of the HDP oxide layers 20A, 20B, 20C and 20D. Note that although not shown in the Figure, the source "drive-in" process will also cause diffusion into the bottom portion of the silicon base 16B of the spacer structure. Appropriate inter-device isolation will be employed at an earlier or later step to prevent this extraneous source diffusion from creating any type of cross-coupling between devices.

[00034] Figure 6 is a cross-sectional diagram of a wafer substrate 600 representative of the wafer substrate 500 of Figure 5 after forming polysilicon gate conductors 24A, 24B, 24C and 24D (gate poly). Gate conductors 24A and 24B are disposed on opposite sides of the first fin 12A (in trenches 10A and 10B, respectively, and atop HDP oxide layers 22A and 22B, respectively), in contact with the gate insulators 22, and are n+ doped. Gate conductors 24C and 24D are disposed on opposite sides of the second fin 12B (in trenches 10C and 10D,

respectively, and atop HDP oxide layers 22A and 22B, respectively), in contact with the gate insulators 22, and are p+ doped. The gate conductors 24A, 24B, 24C and 24D extend vertically partway up the sides of the fins 12A and 12B. Preferably, the gate conductors 24A and 24B are created by forming a "pFET" mask that exposes only desired areas of the nFET device (generally indicated in the Figure as "nFET"), depositing n+ doped polysilicon, etching back to a suitable depth, masking the desired gate outline (nFET litho), and etching with a suitable highly directional etching process, e.g., reactive ion etching (RIE). Then a similar process can be employed to form gate conductors 24C and 24D (i.e., nFET mask, p+ gate poly deposition, etch back, pFET litho, and RIE etch).

[00035] As with the formation of the source conductors 18A-D, those of ordinary skill in the art will immediately appreciate and understand that the order of formation of the gate conductors 24A-D (i.e., n+ first or p+ first) is not critical and the inventive technique is readily adapted to suit either order.

[00036] Figure 7 is a cross-sectional diagram of a wafer substrate 700 representative of the wafer substrate 600 of Figure 6 after implanting drain regions 28A and 28B in top portions of fins 12A and 12B. Preferably, this is accomplished by (1) masking to expose the fin 12A of the inchoate nFET device (and any other similar fin of any other nFET device(s) being simultaneously formed on a larger integrated circuit) then n+ implanting through the mask by any suitable process to form the n+ doped drain region 28A to a depth that extends slightly lower in the fin 12A than the tops of the gate conductors 24A and 24B, then (2) removing the mask and re-masking to expose the fin 12B of the inchoate pFET device (and any other similar fin of any other pFET device(s) being simultaneously formed on a larger integrated circuit) and p+ implanting through the mask by any suitable process to form the p+ doped drain region 28B to a depth that extends slightly lower in the fin 12B than the tops of the gate conductors 24C and 24D. As before, the order of processing (n+ first or p+ first) is not critical.

[00037] Figure 8 is a cross-sectional diagram of a wafer substrate 800 representative of the wafer substrate 700 of Figure 7 after forming nitride sidewall spacers 30. Preferably, the nitride spacers are formed by depositing nitride (by any suitable deposition process), then etching back such that the nitride covers all exposed vertical sidewalls, i.e., the exposed

vertical sidewalls of trenches 10A, 10B, 10C and 10D, gate insulators 22, gate conductors 24A, 24B, 24C and 24D, and nitride caps 14A, 14B and 16A.

[00038] Figure 9 is a cross-sectional diagram of a wafer substrate 900 representative of the wafer substrate 800 of Figure 8 after the formation of silicide gate contact structures 32A, 32B, 32C and 32D; and silicide source contract structures 34A, 34B, 34C and 34D. Preferably, these silicide structures are formed by etching through exposed portions of the HDP oxide layers 20A, 20B, 20C and 20D to expose the polysilicon source conductors 18A, 18B, 18C and 18D, then performing any suitable silicidation process to form silicide gate contact structures 32A, 32B, 32C, and 32D in exposed portions of the gate conductors 24A, 24B, 24C and 24D, respectively and to form silicide source contact structures 34A, 34B, 34C and 34D in the newly exposed portions of the source conductors 18A, 18B, 18C and 18D, respectively. All silicide contact structures (32x and 34x) can be formed essentially simultaneously. Preferably, the silicide contact formation process comprises deposition of the appropriate metal for silicidation (e.g., Cobalt for formation of $CoSi_2$), silicidation by any suitable means (e.g., RTA) and removal of excess metal.

[00039] Figure 10 is a cross-sectional diagram of a wafer substrate 1000 representative of the wafer substrate 900 of Figure 9 after an oxide fill and planarization process. Preferably, a suitable trench-fill technique is employed to overfill the trenches 10A, 10B, 10C and 10D (see Figs 1-7) with oxide fill 36. The oxide fill 36 is then planarized via a CMP process.

[00040] Figure 11 is a plan view of a wafer substrate 1100 representative of the wafer substrate 1000 of Figure 10 after formation of metal source contacts 38A and 38B, drain contacts 40A and 40B and gate contacts 42A and 42B. Preferably, the source contacts 38A and 38B and gate contacts 42A and 42B via a Damascene process whereby openings are formed in the oxide fill extending downward to corresponding silicide contact structures. The openings are filled (overfilled) with metal via a suitable metal deposition process and the metal is polished flush using CMP planarization process. The drain contacts 40A and 40B are preferably formed via a similar Damascene process whereby nitride caps 14A and 14B are selectively etched away to create openings that expose tops of the doped drain regions 28A and 28B, respectively of fins 12A and 12B, respectively. Metal deposition and CMP polishing are used in similar fashion to form the metal drain contacts 40A and 40B. At this

same point, shallow trench isolation 36 is formed around each transistor device using conventional STI techniques. Note that the source contacts 38A and 38B and gate contacts 42A and 42B appear bifurcated. This is because the metal gate contact 42A connects to silicide gate contact structures 32A and 32B on both sides of the fin 12A. Similarly, gate contact 42B and source contacts 38A and 38B connect to respective silicide contact structures on both sides of their respective fins. This is shown and described in greater detail hereinbelow with respect to Figures 12, 13 and 14. Note that the gate contacts 42A and 42B extend only partway across their respective devices. Similarly the source contacts 38A and 38B extend only partway across their respective devices. Also note that the drain contacts 40A only extend laterally a short distance across their respective devices. This facilitates routing of subsequently formed wiring layers that connect to the devices.

[00041] Figure 12 is a cross-sectional view of a wafer substrate 1200 representative of the wafer substrate 1100 of Figure 11 as seen when sectioned at A-A' through the source contacts 38A and 38B. In the Figure, the two legs of bifurcated source contact 38A can be seen extending downward to contact the silicide source contact structures 34A and 34B on either side of fin 12A. Similarly, the two legs of bifurcated source contact 38B are seen extending downward to contact the silicide source contact structures 34C and 34D on either side of fin 12B.

[00042] Figure 13 is a cross-sectional view of a wafer substrate 1300 representative of the wafer substrate 1100 of Figure 11 as seen when sectioned at B-B' through the drain contacts 40A and 40B. In the Figure, the drain contacts 40A and 40B can be seen extending downward to contact respective drain regions 28A and 28B in respective fins 12A and 12B.

[00043] Figure 14 is a cross-sectional view of a wafer substrate 1400 representative of the wafer substrate 1100 of Figure 11 as seen when sectioned at C-C' through the gate contacts 42A and 42B. In the Figure, the two legs of bifurcated gate contact 42A can be seen extending downward to contact the silicide gate contact structures 32A and 32B on either side of fin 12A. Similarly, the two legs of bifurcated source contact 42B are seen extending downward to contact the silicide source contact structures 32C and 32D on either side of fin 12B.

[00044] One alternate embodiment of the inventive vertical Fin-FET device employs a "fat drain" structure that improves drain contact resistance. This is shown and described with respect to Figure 15.

[00045] Figure 15 is a cross-sectional view of a wafer substrate 1500 representative of the wafer substrate 1100 of Figure 11 as seen when sectioned at B-B' through "fat-drain" contacts 40A and 40B. In the Figure, the drain contacts 40A and 40B laterally overextend their respective fins 12A and 12B. The "fat-drain" contacts are preferably formed by masking off the desired drain contact profiles, performing a controlled nitride/oxide etch, disposing thin Si epitaxial layers 44A, 44B at the bottoms of the openings thus formed, then forming the metal drain contacts 40A and 40B by metal deposition and CMP polishing as described hereinabove.

[00046] In some applications, it may be desirable for the source contacts to connect only to one side of their respective fin. Figure 16 is a plan view of a wafer substrate 1600 similar to the wafer substrate 1100 of Figure 11 except that the source contacts 38A and 38B are formed on only one side of their respective fins (12A, 12B).

[00047] The gate contacts 42A and 42B are bifurcated to connect in common to silicide gate contact structures on both sides of their respective fins 12A, 12B (see Figures 11, 14). In some applications, it may be desirable to provide separate gate contacts to the gate conductors on each side of the Fin-FET device, thereby creating a Fin-FET with multi-gate voltage control. This is shown and described with respect to Figure 17.

[00048] Figure 17 is a plan view of a wafer substrate 1700 similar to the wafer substrate 1100 of Figure 11 except that instead of forming bifurcated gate contacts (see 42A, 42B, Fig. 11) the legs of the gate contacts are kept separate, thereby providing separate gate contacts 42AA, 42AB, 42BA and 42BB connecting to respective silicide gate contact structures 32A, 32B, 32C and 32D (see, e.g., Figs. 10, 14). This permits the gate contacts on each side of their respective Fin-FET devices to be controlled independently, thereby creating multi-gate vertical Fin-FETs.

[00049] In applications that require higher drive currents, multi-fin versions of the vertical Fin-Fet structure can be formed. All gate contacts are connected in parallel, all drain contacts are connected in parallel and all source contacts are connected in parallel, effectively

creating an array of parallel-connected vertical fin-FETs with effective channel width multiplied by the number of fins employed, and correspondingly improved drive current capability. Connecting to "left side" and "right side" silicide gate contact structures separately creates a dual-gate version of the multi-fin vertical fin-FET. A multi-fin vertical Fin-FET device is shown and described with respect to Figure 18.

[00050] Figure 18 is a cross-sectional view of a wafer substrate 1800 on which a multi-fin version of the vertical Fin-FET device has been formed prior to metal contact formation. Those of ordinary skill in the art will immediately understand that the processing steps required to create the multi-fin vertical finFET are essentially the same as those described hereinabove for creating single-fin devices. Three thin vertical fins 112A, 112B and 112C are formed, doped polysilicon source conductors 118A, 118B, 118C and 118D are formed alongside the fins 112A, 112B and 112C. The doping of the source conductors should be appropriate to the type of device being formed (n+ for nFET, p+ for pFET). HDP oxide insulating layers 120A, 120B, 120C and 120D are formed atop source conductors 118A, 118A, 118C, and 118D, respectively. Gate insulators, gate conductors and nitride sidewall spacers are all formed in similar fashion to that described hereinabove. Silicide gate contact structures 132A, 132B, 132C, 132D, 132E and 132F are formed in top surfaces of the gate conductors on each side of the fins 112A-112C and silicide source contact structures 134A, 134B, 134C, 134D, 134E and 134F are formed in top surfaces of the source conductors 118A, 118B, 118C, 118D, 118E, and 118F, respectively. An oxide trench fill 136 is deployed and planarized as described hereinabove. Subsequent processing steps form metal gate, source and drain contacts in similar fashion to that described hereinabove for single-fin devices.

[00051] It is generally assumed that the present inventive vertical Fin-FET device will be applied to larger CMOS (complementary MOS) circuits. It is fully within the spirit and scope of the present invention to do so. Accordingly, the descriptions hereinabove with respect Figures 1-17 have shown nFET and pFET devices side-by-side. Typically these devices will be part of a CMOS circuit, which may in turn be part of a larger integrated circuit device employing many such CMOS circuits. Further, individual nFET and pFET versions of the inventive vertical Fin-FET can be employed in any type of circuit (including non-complementary circuits) on an integrated device with or without other CMOS circuits.

Those of ordinary skill in the art will understand that through appropriate masking, any desired combination of nFET and pFET vertical Fin-FET devices can be created.

[00052] In the description of the inventive vertical Fin-FET and its various embodiments, specific reference has been made hereinabove to "drain contacts" and "drain regions" generally located at top portions of the fins and "source contact structures", "source conductors" and "source regions" generally located at bottom portions of the fins. Those of ordinary skill in the art will understand that as with many MOS devices, the designations "source" and "drain" can be interchanged, thereby reversing the presumed direction of current flow within the transistor, although performance may or may not be identical in both directions.

[00053] Those of ordinary skill in the art will also appreciate and understand that any of the various aspects and embodiments of the inventive technique can be used alone or in combination (e.g., dual-gate, single-side source, fat drain, multi-fin, etc.). For example, a dual-gate, multi-fin device has already been described. By way of further example, the "fat drain" structure can also be employed in dual-gate and/or multi-fin variants of the vertical Fin-FET.

[00054] Processing steps as described hereinabove have generally been presented in "nFET first order" whereby nFET structures are formed first, followed by pFET structures. Those of ordinary skill in the art will immediately understand that the order of processing is not critical, and that the inventive technique is readily adapted to either order of processing. Further, if only nFET devices or pFET devices are required, some intermediate steps can be eliminated.

[00055] The vertical Fin-FET device of the present invention provides several advantages in addition to the high-density advantages that derive from its vertical orientation. The "double-gate" feature is an inherent feature of the device and provides a significant advantage in offering improved drive current. Drive current can be further enhanced by creating multiple-fin versions of the vertical Fin-FET as described hereinabove with respect to Figure 18. The same process steps can be used to create both single-fin and multi-fin devices, so there is no processing penalty in mixing them on a single integrated circuit device.

[00056] The present invention has been described hereinabove specifically with respect to silicon-based semiconductor technology. Those of ordinary skill in the art will immediately understand that similar techniques can be employed to produce equivalent structures having vertically oriented transistor "fin" bodies with vertical current flow using other semiconductor technologies. The description in terms of silicon-based semiconductor technology hereinabove should be viewed as exemplary rather than limiting.

[00057] Although the invention has been shown and described with respect to a certain preferred embodiment or embodiments, certain equivalent alterations and modifications will occur to others skilled in the art upon the reading and understanding of this specification and the annexed drawings. In particular regard to the various functions performed by the above described components (assemblies, devices, circuits, etc.) the terms (including a reference to a "means") used to describe such components are intended to correspond, unless otherwise indicated, to any component which performs the specified function of the described component (i.e., that is functionally equivalent), even though not structurally equivalent to the disclosed structure which performs the function in the herein illustrated exemplary embodiments of the invention. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several embodiments, such feature may be combined with one or more features of the other embodiments as may be desired and advantageous for any given or particular application.